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Half Swing Clocking Scheme at 45nm

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ABSTRACT
Achievement of high processor speed with low power consumption is an elemental factor in processor technology, especially for hand-held devices. The need for low power has caused a major paradigm shift where power dissipation has become a important consideration as performance and area. In CMOS circuits, dynamic power consumption is proportional to the transition frequency, capacitance, and square of supply voltage. Consequentially, lowering supply voltage delivers significant power savings compromising the speed of processor. Large portion of the total power is consumed in the clocking circuitry in embedded processor technology. So clock power can be reduced using half swing of clock scheme which will cut down the power dissipation and minimum speed degradation. In Digital circuits by using double-edge triggered flip flops (DETFFs), the clock frequency can be significantly reduced ideally, in half while preserving the rate of data processing. Using lower clock frequency may translate into considerable power savings for the clocked portions of a circuit, including the clock distribution network and flip-flops. The designing is based on 45nm process technology.
Keywords: Clock power, CMOS, DETFF.

I. INTRODUCTION

In recent ages major interest of designers were on area, performance, cost, reliability, and power. Power is most crucial factor of the embedded processor technology. Power distribution in embedded processor differs from product to product but due to the large capacitance and high switching activity clock system dissipates enormous portion of power which is about 18-43% of total circuit. One of the main reasons for enormous power consumption in the clock system is that the transition probability of the clock is 100% while in ordinary logic it is about one-third on average.

Many power reduction techniques have been introduced in random logic but techniques are useful for all random logic circuits which does not help to degrade power consumption Consequently, in order to achieve low-power designs, it is relevant to degrade the clock system power and for reducing the clock system power, it is beneficial to reduce a clock voltage swing. By using half swing clocking scheme we can achieve significant reduction in power consumption. Proposed half swing clocking scheme causes the minimum speed degradation because voltage swing is reduced only for clocking circuitry but the random logic circuits in critical path are provided with full supply voltage as a result significant power reduces with minimal speed degradation.

II. HALF SWING CLOCKING SCHEME

Fig 2 shows the proposed half-swing clocking technique which is compared with a conventional technique.

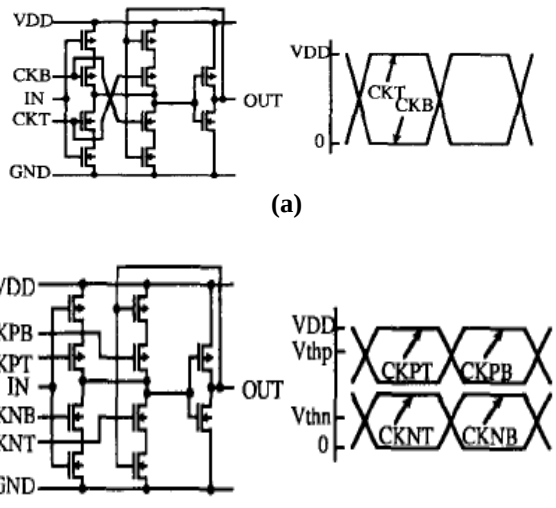

Fig.2 Concept of half swing clocking scheme.(a) conventional clocking scheme (b) half swing clocking scheme.

In Fig. 2(a) two full-swing clocks is being gated to a conventional latch. The voltage swing of the clock is reduced to half VDD which will degrade the clocking power. The proposed technique as shown in

Fig. 2(b), uses two separate clock signals for NMOS and PMOS transistors, respectively. For NMOS's clock swings from zero to half VDD, and for PMOS's the clock swings from VDD to half VDD. The power degradation by half swing clocking circuitry is decreased to 25% of conventional clocking circuitry. Half swing clock driver provides two half swing clock signals as discussed above and generate half VDD voltage by itself.

III. HALF SWING CLOCK DRIVER

Non overlapping two phase clock system is used for designing latches. Two pairs of complementary clock phases $\Phi_{1,}/\bar{\Phi}_{1,}$& $\Phi_{2,}/\bar{\Phi}_{2,f}$ is required for designing C^2MOS latches and transmission–gates (tmg) . $\Phi_{1,f}$ and $\Phi_{2,f}$ controls the NMOS gates, whereas $\bar{\Phi}_{1,f}$ and $\bar{\Phi}_{2,f}$ are connected to PMOS gates. Figure shows the two complementary full swing phases and a C^2MOS latch.

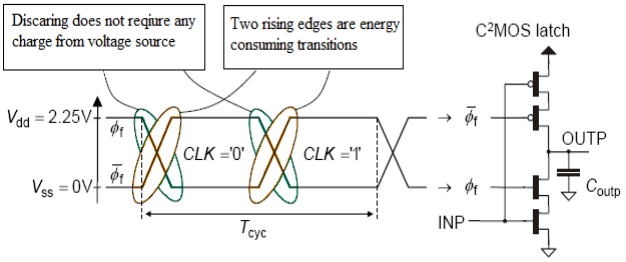

Fig. 3.1 Complementary full swing clocking

As there is four phases of clock and the energy consumption per clock period is determined by two full-swing transitions. Thus two discharging edges does not require any charge from voltage source and two rising edges of clock require charge from voltage source. The power consumed by the clock is given by

$$P_{clk,f} = C_{clk,f} \cdot V2dd \cdot f_{clk} \quad (1)$$

Where $C_{clk,f}$ is the total capacitance of the four clock phases, V_{dd} is power supply voltage and f_{clk} is the switching frequency of clock.

Figure 3.2 shows two complementary phases Φ_h / $\bar{\Phi}_h$ of half swing clocking scheme. In the Low to High transition (LH) of Φ_h can be obtained by connecting it to $\bar{\Phi}_h$,which does not require any charge from the voltage source. The energy dissipating by $\bar{\Phi}_h$ is used by Φ_h .So shorting these two complementary phases no energy requires from voltage source. The only energy consuming state is Low to High transition of $\bar{\Phi}_h$

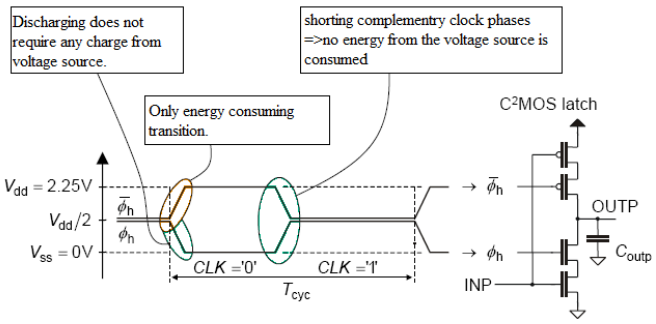

Fig. 3.2 Complementary half swing clocking[11]

Half swing clock drivers are suggested in reference [2] [5] is shown in figure 4.

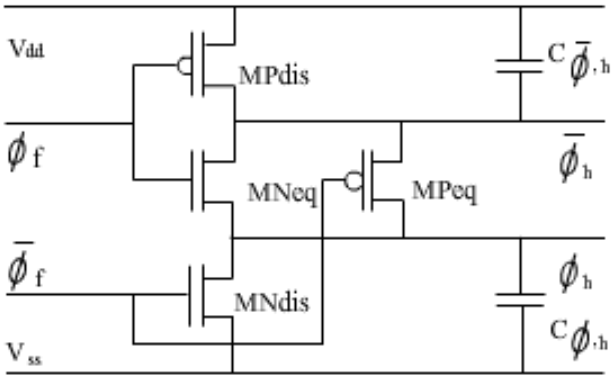

Fig.4 Half swing clock driver

Half swing clock driver generates half swing clock and half V_{dd} voltage which is comprise of four transistors and two capacitors. When voltage at phase of full swing clock $V_{\Phi f}$ = 0, transistor MPeq and MNeq are off, Φ_h and $\bar{\Phi}_h$ are discharge by MNdis and MPdis to V_{ss}=0 and V_{dd} respectively. When $V_{\Phi f}$ =V_{dd}, these MNdis and MPdis are off and MPeq and MNeq are short circuit Φ_h and $\bar{\Phi}_h$, which met at potential V_{eq}.

$$Veq = \frac{C_{\bar{\Phi}h}}{C_{\Phi,h}+C_{\bar{\Phi}h}} Vdd \quad (2)$$

With $C_{\bar{\Phi}h} = C_{\Phi,h}$,V_{eq} become equal to $V_{dd}/2$.

IV. FLIP-FLOP

Flip-flop is a is a clocked storage elements, which can be used to store state information and also store the values which is applied to their inputs. Flip flops and latches are most frequently used element in digital systems. A latch is level sensitive. It is transparent and propagates its input to the output during one clock phase (clock low or high), while holding its value during the other clock phase. A flip-flop is edge triggered. It captures its input and propagates it to the output at a clock edge (rising or falling), while keeps the output constant at any other time. In synchronous system, they are the starting and ending points of signal delay paths, which decide the maximum speed of the systems. Typically they are

consuming large amount of power because they are clocked at the system operating frequency. The clock power of a high performance processor dominant the total power dissipation. A large portion of the clock power is used to drive sequential elements such as flip flop and latches. Reducing the clock power dissipations of the flip flop and latches is thus important technique for the total chip power conservation.

A. SINGLE & DOUBLE EDG TRIGGERED FLIP- FLOP

Double-edges triggered (DET) and single-edge triggered (SET) flip-flops are edge-sensitive devices. Data storage in these flip-flops occurs at specific edges of the clock signal. The single-edge triggered (SET) flip-flops are shown in figure, has two D latch .The first latch is called the master and the second is slave.

When the clock is 0, the output of the inverter is 1. The slave latch is enabled and its output Q is equal to the master output.

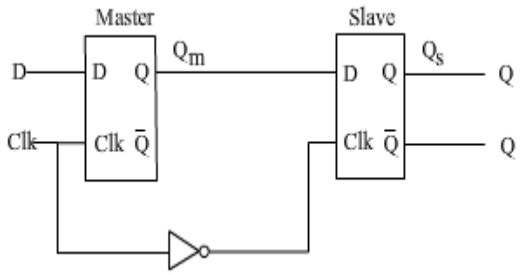

Fig. 5 single-edge triggered (SET) flip-flops

The master latch is disabled because Clk =0 .When the input pulse changed to the logic 1 level, the data from external D input is transferred to the master. The slave, however is disabled as long as clock remains in the level 1(high).Thus ,the output of the flip flop can changed only during the transition of the clock from 1 to 0.

Double-edge triggered flip-flops sample the input data at both the rising and the falling edges of the clock signal during each period of the clock signal.

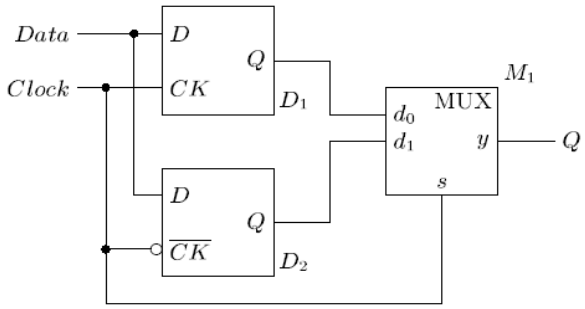

Fig. 6 Double edge triggered (DET) flip-flops

When the clock signal Clock is high the latch D_1 is transparent and *M*1 multiplexes to the global output Q the value stored in the latch D_2 Similarly, when the clock signal Clock changes to low, the latch D_2 becomes transparent, and the value Stored in D_1 is multiplexed to the global flip-flop output Q.

V. SIMULATION AND RESULTS

The tool used is Tanner EDA version 14.1.Tanner tool is VLSI design tool used for analysis and simulation of electronic circuits. Technology used is 45nm.45nm FET process parameter file is included in T-spice file for simulations. The width of PMOS is 2.1u and NMOS_1 (MNeq) is 0.5u and NMOS_2 (MNdis) is 1.34um.The value of capacitance $C_{\Phi h}$ = 1pF and $C_{\Phi,h}$=1pF.

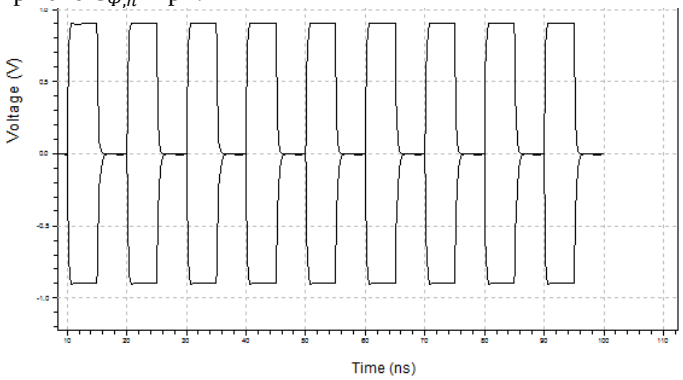

Fig. 7 simulation result for half swing clock driver

The resizing of latch transistor is necessary to restore the shape and timing of output edge. Reduced clock voltage leads to reduced drain current causes longer latch delay. Resizing channel width of latch transistors is necessary. C^2MOS latch waveform is shown in figure 8.

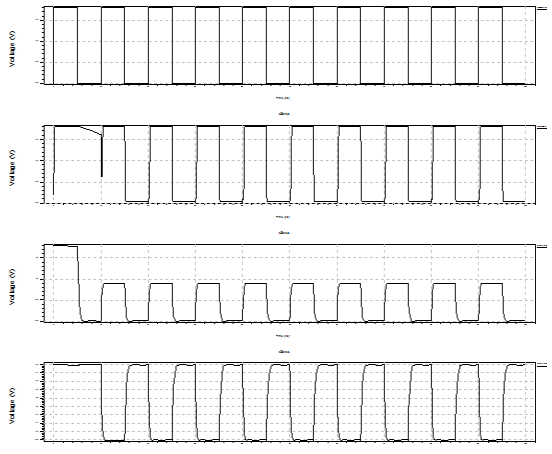

Fig .8 simulation result for C^2MOS latch for half swing clock

The figure 9 shows output waveform for SET Flip Flop using C^2MOS latch. The width of PMOS is equal to 2.1um and NMOS is equal to 45nm.

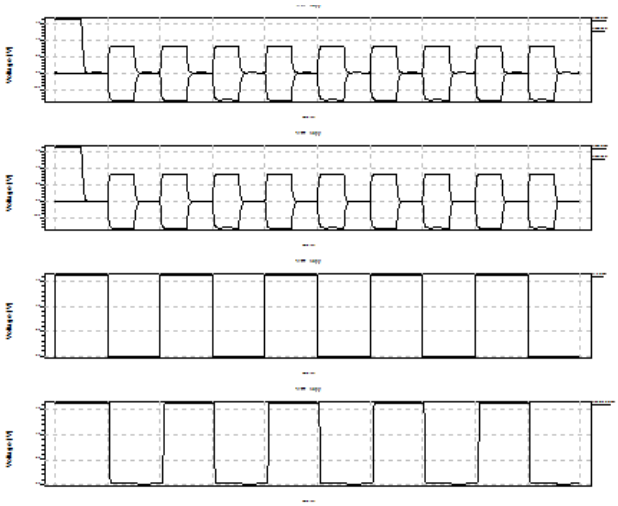

Fig .9 simulation result for SETFF using C^{2}MOS latch for half swing clock

Input to output delay for SETFF T_{PLH}=622.07ps.The waveform of DET flip flop with C^{2}MOS latch using half swing clock is shown in figure 5.9 the width of PMOS is 2.1µm and NMOS is 45nm and the length will be equal to 45nm.

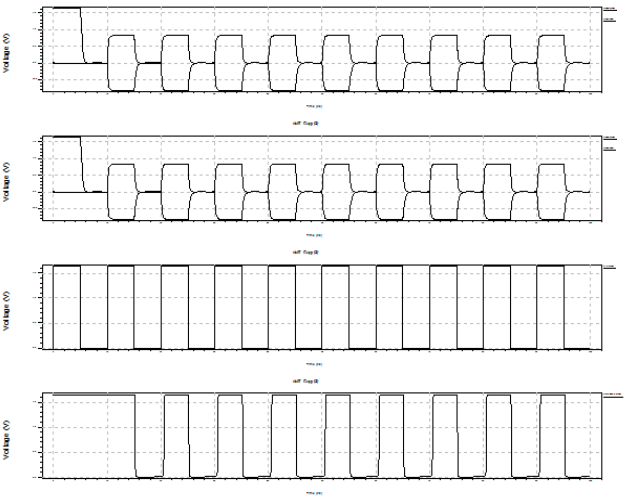

Fig .10 Simulation result for DETFF using C^{2}MOS latch for half swing clock

Input to output delay for DETFF is T_{PLH}=582.58ps.In the comparison table power and delay are calculated for SETFF and DETFF at the 45nm technology. In comparison to 45nm and 180nm technology, it is found that there is a significant raise of 16% power consumption in case of 45nm technology over 180 nm technology. This has resulted into significant power reduction with minimal speed degradation.

Flip Flop	Technology	Power (watt)	Delay (rise)sec.
DETFF	45nm	8.3881×10^{-4}	582.58p
SETFF	45nm	4.281×10^{-4}	622.07p
DETFF	180nm	1.00694×10^{-3}	674.07p
SETFF	180nm	1.964×10^{-3}	840.96p

Table.1 Comparison table for DETFF based on 45nm and 180 nm technology

VI. CONCLUSION

This design is an attempt to develop a low power and voltage DETFF. Large portion of the total power is consumed in the clocking circuitry in embedded processor technology, so Half-swing clocking system technique reduces clock power greatly. Clocked C^{2}MOS latches is suitable for half-swing clock technique , when Transmission-gates latch is being used with the half swing clock it produces a kinked output with half swing clock. Double edge triggered flip flop using half swing clock results in substantial power reduction. Double edge triggered flip flop as compared to single edge triggered flip-flop responds to both clock edges, reducing clock frequency to half in order to achieve the same computation output. Clock distribution turns out to be a major source of power consumption in a synchronous computation system resulting in overall power reduction which is beneficial to a great extent. It has been shown that the usage of DETFFs in processor technology is beneficial in low power, low voltage and high speed applications. Design of DETFF on 45nm processor technology have 16% of improvement over the 180nm technology.

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